

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
UNIVERSITY EXAMINATION CENTER, KAKINADA- 533003**

M.TECH II SEMESTER (R09)- SPECIAL SUPPLEMENTARY EXAMINATIONS, MAY - 2018

TIME TABLE

TIME: 2:00PM TO 5:00 PM


BRANCHES AND SPECIALIZATIONS	21.05.2018 (Monday)
MECHANICAL MACHINE DESIGN (15)	Experimental Stress Analysis (D1502)

NOTE: (i) ANY OMISSION OR CLASHES IN THIS TIME TABLE MAY PLEASE BE INFORMED TO THE CONTROLLER OF EXAMINATIONS, JNTUK, KAKINADA IMMEDIATELY.

(ii) EVEN IF GOVERNMENT DECLARES HOLIDAYS ON ANY OF THE ABOVE DATES, THE EXAMINATIONS SHALL BE CONDUCTED AS USUAL.

(ALL The above Examination will be conducted at Kakinada only)

Date: 13-04-2018


Controller of Examinations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
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BRANCHES AND SPECIALIZATIONS	21.05.2018 (Monday)	22.05.2018 (Tuesday)	23.05.2018 (Wednesday)	24.05.2018 (Thursday)	25.05.2018 (Friday)	26.05.2018 (Saturday)
CSE COMPUTER SCIENCE & ENGINEERING (58)	Secured Database Applications Development (D5810)	Data Warehousing and Data Mining (D5809)	<u>Electives</u> Object Oriented Software Engineering (D5803)	<u>Elective</u> Human Computer Interaction (D5808)	Computer Networks (D5802)	Web Technologies (D5807)

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EEE POWER ELECTRONICS (43)	Digital Signal Processing and Applications (D4304)	Switched Mode Power conversion (D4301)	Power Electronics Control of AC Drives (D4302)	<u>Electives</u> 1.Digital control Systems (D4305)	<u>Electives</u> 1.Power Quality Management (D4307)
EEE POWER & INDUSTRIAL DRIVES (42)	Digital Signal Processing and Applications (D4304)	----	----	----	----
EEE POWER ELECTRONICS AND POWER SYSTEMS (99)	Advanced Power System Protection (D5604)	----	----	----	----

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ECE EMBEDDED SYSTEMS (55)	Low Power VLSI Design (D5505)	-----	Algorithms for VLSI Design Automation (D5501)	----
ECE VLSI D & VLSID/VLSI (72)/(57)	Low Power VLSI Design (D5505)	-----	Algorithms for VLSI Design Automation (D5501)	DSP Processor & Architecture (D3803)
ECE VLSI & EMBEDDED SYSTEMS /ES & VLSI DESIGN (68)/(81)	Low Power VLSI Design (D5505)	CPLD and FPGA Architecture and Applications (D5506)	Algorithms for VLSI Design Automation (D5501)	-----

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N. Mohan Rao
Controller of Examinations